Applicant: Koujiro Kameyama et al. Attorney's Docket No.: 14225-046001 / F1040123US00

Serial No.: 10/812,454 Filed : March 30, 2004 Page : 5 of 8

# Amendments to the Drawings:

The attached replacement sheet of drawings includes changes to FIG. 7 and replaces the original sheet including FIG. 7.

As required by the Examiner, Figure 7 has been labeled as Prior Art.

Attachments following last page of this Amendment:

Replacement Sheet (one page)

Applicant: Koujiro Kameyama et al. Attorney's Docket No.: 14225-046001 / F1040123US00

Serial No.: 10/812,454 Filed: March 30, 2004

Page : 6 of 8

### **REMARKS**

Claims 1-8 have been canceled and replaced by claims 18-22. Claims 9-17 previously were withdrawn as the result of a restriction requirement.

## **Drawings**

As required by the Examiner, FIG. 7 has been labeled with the legend "Prior Art."

## Inventors' Declaration/Oath

The Office action states that the "Oath appears to contradict the claim of foreign priority (see page 2 of Oath filed 7/6/04 (Priority not claimed")." Applicant respectfully disagrees.

The Declaration executed by the inventors states (page 1), in part, as follows:

I hereby claim foreign priority under Title 35, United States Code, Section 119(a) (d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application for which priority is claimed.

It should be clear that applicant claims priority from the foreign application listed at the top of page 2 of the Declaration *unless the box is checked*, which, in this case, it is not. Accordingly, it is respectfully submitted that a new inventors' Declaration is not required.

### Claims

Independent claims 18 recites a semiconductor device that includes a semiconductor element, a first conductive means, a penetrating region extending from the front surface to the back surface of the semiconductor element in a manner substantially vertical to the front and back surfaces, a second conductive means located inside the penetrating region and electrically

Applicant: Koujiro Kameyama et al. Attorney's Docket No.: 14225-046001 / F1040123US00

Serial No.: 10/812,454 Filed: March 30, 2004

Page : 7 of 8

ì

connected to the first conductive means, and a cover that is transparent to a light and is located on the front surface of the semiconductor element.

An example is illustrated in FIG. 1B in which the semiconductor element is identified by 11, the first conductive means is identified by 15 and the second conductive means is either of the hatched areas extending vertically through the semiconductor element 11.

In the Office action, original claims 1-8 were rejected in view of JP 2000-173766 or the Badehi patent.

JP 2000-173766 discloses, for example in FIG. 7(b), a device on a transparent substrate 1. The device includes an electroluminescence layer 5 and pixel electrodes 4 connected to selection drive circuits 2. An insulating layer is located between the electroluminescence layer 5 and the substrate 1. A counter electrode, identified by 6, is surrounded by a resin seal layer 33.

The Badehi patent discloses, for example in FIG. 2A, a microlens array 100 on a substrate 102. Spacers 116 separate the mircolens array from a transparent packaging layer 114 that covers the array. Conductive pads 112 electrically connect the substrate 102 to bumps 110 by way of electrical contacts 108 extending along the side of the package. Reference numerals 104 and 118 identify areas of epoxy. Below the epoxy 104 is a glass packaging layer 106. Neither of those references, taken alone or together, discloses or suggests the subject matter of claims 18-22. For example, those references do not disclose or suggest "a penetrating region extending from the front surface to a back surface of the semiconductor element in a manner substantially vertical to the front and back surfaces of the semiconductor element, wherein the penetrating region is located over the first conductive means and away from side surfaces of the semiconductor element" and "a second conductive means located inside the penetrating region and electrically connected to the first conductive means."

Applicant submits that the pending claims should be allowed.

ł

Applicant: Koujiro Kameyama et al.

Serial No.: 10/812,454 Filed: March 30, 2004

Page

: 8 of 8

Attorney's Docket No.: 14225-046001 / F1040123US00

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: /1/9/05

Samuel Borodach Reg. No. 38,388

Fish & Richardson P.C. Citigroup Center 52nd Floor 153 East 53rd Street New York, New York 10022-4611

Telephone: (212) 765-5070

Facsimile: (212) 258-2291

30244518.doc